Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) MAR 2 9 2004 Sheet 1 of ACCEPTAGE

January 25, 2001	DECELV
Rumynin, Dmitriy	RECEIV
2124	MAR 3 1 2
Malzahn, David	MAN-O I C
	Rumynin, Dmitriy 2124

US PATENT DOCUMENTS							
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate	
2	US-2002/0026465	02/28/2002	Rumynin, D, et al.	708	210	01/25/2001	
Alle	US-2002/0078110	06/20/2002	Rumynin, D , et al.	708	210	07/27/2001	
Afth	US-5,964,827	10/12/1999	Ngo, Hung C., et al.	708	710	11/17/1997	
ST	US-6,175,852B1	01/16/2001	Dhong,, et al.			07/13/1998	
EX	US-6,269,386B1	07/31/2001	Siers, , et al.	708	710	10/14/1998	

Attorney Docket No: 1365.039US1

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T²

	OTHER	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
-		BEDRIJ, O. J., "Carry-Select Adder", IRE Trans., EC-11, (June 1962),340-346	
4		KNOWLES, S., "A Family of Adders", Proc. 14th IEEE Symp. on Computer Arithmetic, (1999),30-34	
221		KOGGE, P. M., et al., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations", <u>IEEE Trans. Computers</u> , Vol. C-22, No. 8, (Aug. 1973),786-793	
A)		LADNER, RICHARD E., et al., "Parallel Prefix Computation", <u>Journal of ACM</u> , <u>Vol. 27, No. 4, (Oct. 1980)</u> ,831-838	
		LING, HUEY, "High-Speed Binary Adder", <u>IBM Journal of Research and</u> <u>Development, Vol. 25, No. 3, (1981),156-166</u>	
Like		SKLANSKY, J., "Conditional-Sum Addition Logic", <u>IRE Trans., EC-9</u> , (June 1960),226-231	
24		WEINBERGER, A., et al., "A Logic for High-Speed Addition", Nat. Bur. Stand. Circ., 591, (1958),3-12	

D. H. Malzukn

EXAMINER

4/26/04 **DATE CONSIDERED**